IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Confirmation: 4533

Yasuhiro WAKIMOTO Art Unit: 2186

Serial No.: 09/652,023 Examiner: W. Choi

Filed: August 31, 2000 Docket No.: 108391-00011

For: MICROPROCESSOR AND MEMORY DEVICE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

March 7, 2003

Dear Sir:

In reply to the Office Action dated October 21, 2002 and prior to initial examination of the attached Request for Continued Examination (RCE), please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claim 18 without prejudice or disclaimer, and amend claims 1, 4, 7 and 12 as follows:

1. (Twice Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module